

# PUSSEE



**Paradigm Unifying System  
Specification Environments for  
proven Electronic design**

<http://www.keesda.com/pussee>

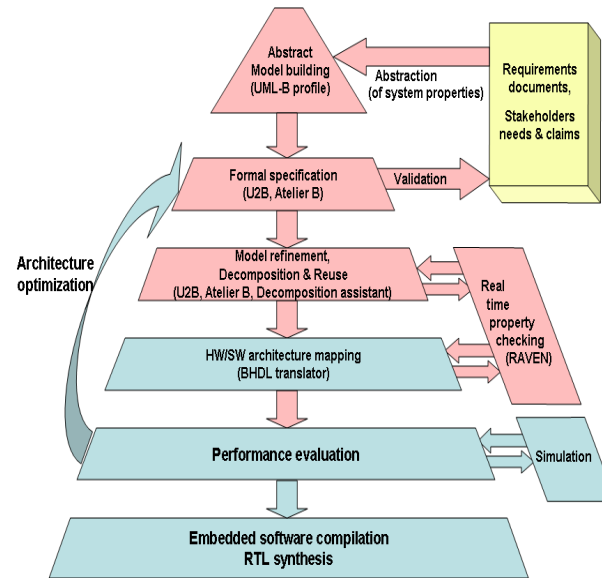


**Contract No.: IST-2000-30103**

## The Project

The PUSSEE project introduces two key aspects, *reusability* and *formal proof of system properties*, that enable the development of highly reliable systems in significantly reduced time-to-market windows. Reusability, although quite popular in the software world, has not

gained the required acceptance in the domain of embedded systems. Its concept is simple, but its actual use in practice is rather limited.



Despite the plethora of emerging methodologies, only a small fraction of them efficiently support the integration of reusable system parts. The approach proposed by PUSSEE takes into account the reuse of existing components at the various levels of the development cycle. During the early design stages UML reuse mechanisms are employed, through the use of a UML-B specialized profile.

The second significant concept introduced by PUSSEE, is the use of the B language

for proving the properties of the system under development. The formality of B complements the lack of formal semantics, which is one of the major drawbacks of UML. In this way, the two languages are jointly used for the development of complex systems, the behavior of which can be formally proven during early development stages.

As a result, design flaws and potential inefficiencies are discovered early enough to be fixed at minimum cost. Moreover, the reusability of B abstract machines at any level of refinement, with preservation of the integrity of the proven system specification, introduces a breakthrough in the reusability practice, opening the door to system decomposition and interface-based design.

## Technical approach

The core technology delivered by PUSSEE project relies on techniques for the definition of component interfaces and their interconnections based on a combination of UML and B. The project will deliver a technology that allows for the development of hardware and software from high-level definitions, thus providing a uniform approach to the development of embedded systems. It also exploits technologies already used by the embedded systems industry, such as SystemC for simulation and VHDL for synthesis, by providing links between these and UML and B.

## Key Issues

- ◆ Definition of the synergy between UML and B
- ◆ Tools support for verification and stepwise formal refinement
- ◆ Definition of a B hardware interpretation and associated automatic tools
- ◆ Elaboration of reusable components for both system specification (UML and B models) and system development (virtual components)
- ◆ Interface based design allowing sub-systems composition

## Impact

The PUSSEE project proposes an evolutionary rather than a revolutionary approach to improve the embedded systems development process. Rather than proposing an alternative method, PUSSEE enhances the analysis that can be performed during design by combining UML with B so that existing skills and know-how can continue to be used while being extended.

A consequent impact is the delivery of a uniform approach to component definition, by supporting rigorous analysis of embedded components and component assemblies through the automated proof technology. This technology is integrated with existing design technologies such as UML and VHDL and tailored to the needs of embedded system design. The feasibility of

the PUSSEE approach has been verified through real world case studies borrowed from the telecom and automotive domain.

## Results

- ◆ A tool linking UML tools to Atelier-B by providing translations between UML diagrams and B.
- ◆ A prototype tool that translates B to SystemC and VHDL
- ◆ A method of complementing B to better support specification, refinement and code generation of systems with real-time properties.
- ◆ A method with tool support for interface based design (VSIA/SLIF) and integration of legacy components

Results are being commercialised and disseminated through conferences, courses and web pages.

**Start of Project:** January 2002

**End of Project:** January 2004

## List of participants

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